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10/026,459	12/27/2001	Yasushi Nagata	P21847	7837

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EXAMINER
TAKAOKA, DEAN O

ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/026,459	Applicant(s) NAGATA ET AL.	
	Examiner Dean O Takaoka	Art Unit 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,11-13 and 15-18* is/are rejected.

7)☒ Claim(s) *6,7,9,10,14 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

i) The character "あ" after the word "electrodes" (page 6, line 10) is not understood.

ii) The statement of "incorporation by reference" to the foreign application (page 27, line 14-16) is only required in the declaration and with submission of the priority document. Since the requirements for priority have been satisfied, "incorporation by reference" is understood and not required in the specification, thus is requested to be removed from the specification.

Appropriate correction is required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore the following below must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

i) "spaced by a given distance" (claim 6).

It does not appear that any spacing is shown between the high frequency terminals and the outer edge of the multi-layer assembly (Figs. 4 and 5).

ii) "wherein the high-frequency terminals are equipped with solder balls" (claim 12).

The high-frequency terminals equipped with solder balls does not appear to be shown in any figures.

iii) "a circuit board...wherein lands provided on said circuit board are arranged smaller in size than the high-frequency terminals of said high-frequency switching module" (claim 14).

The circuit board with smaller land size than the module does not appear to be shown in any figures.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The applicant is required to provide a copy of the drawings with proposed drawing changes marked in red ink as required by 37 CFR 1.121(d).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 3, 8, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi-Kesheh et al. (U.S. Patent No. 5,513,382) and further in view of Shaprio (U.S. Patent No. 5,834,994).

Claim 1:

Agahi-Kesheh et al. shows a high-frequency switching module primarily including a switching circuit (106 – Fig. 1) and filtering circuit (comprising elements 148, 158 and 164 forming a well-known pi filter within switching circuit 106, the circuits best illustrated

in Figs. 1-3) comprising: a multi-layer assembly having a plurality of dielectric sheets of layers placed one over the other (Fig. 4); a plurality of high-frequency terminals provided on the outer surfaces of the multi-layer assembly (Fig. 5F); the switching circuit (142, 176 – Fig. 1) formed in the layers of the multi-layer assembly, having one end connected to a first high-frequency terminal (e.g. 142 connected to 112) of the plurality of high-frequency terminals; the filtering circuit (148 et al. – Fig. 1) formed in the layers of the multi-layer assembly, having one end connected to the other end of the switching circuit (124) and the other end connected to a second high-frequency terminal (218) of the plurality of high-frequency terminals, where the high-frequency terminals are provided on the mounting side surface of the multi-layer assembly (399 – Fig. 5F).

Agahi-Kesheh et al. does not show where lateral sides of the multi-layer assembly are not provided with any electrode for the high-frequency terminals.

Shapiro (Figs. 1 – 6) shows a high-frequency module where lateral sides (106, 108, 110, 112) are not provided with any electrode (sides disclosed as unmetallized; col. 2, lines 10 – 23) for high frequency terminals (where I/O terminals are on the bottom surface of 104 – Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified bottom layer I/O terminals disclosed by Agahi-Kesheh et al. using the bottom side I/O terminals design including ground plane disclosed by Shapiro. Such a modification would have realized the advantageous benefit of being easily surface mountable and providing a ground plane with the advantage of both isolation between the input and out put and sufficient harmonic

rejection (Shapiro – col. 2, lines 33-42), thus suggesting the obviousness of the modification.

Claim 2:

Where the connection between one end of the switching circuit and the first high-frequency terminal and the connection between the other end of the filtering circuit and the second high-frequency terminal are implemented through corresponding via-holes provided in the multi-layer assembly (vias shown by Agahi-Kesheh et al. in Figs. 5A-F).

Claim 3:

Where the multi-layer assembly has a grounding electrode provided on a dielectric sheet closer to the mounting side surface than from the filtering circuit (where the substituted ground plane of Shapiro, GP2 occurs on the bottom mounting surface, thus obviously closer to the mounting side surface than from the filtering circuit).

Claims 4 and 5:

Agahi-Kesheh et al. and Shapiro teach the high-frequency switching module (discussed above in the reasons for rejection of claim 1 above) including terminals arranged extending along the outer edge of the mounting side surface.

Agahi-Kesheh et al. and Shapiro do not show where the electrode width at the outer edge is greater than at the inner region.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have either used the rectangular terminals disclosed by Agahi-Kesheh et al. and Shapiro or the terminals where the electrode width at the outer edge is greater than at the inner region. Such use of either terminal shape would have been

functionally equivalent since the shape of either terminal would provide the same conductive connection function thus suggesting the obviousness of the use of either terminal shape.

Claim 8:

Where the multi-layer assembly has a rectangular four-sided outer shape and has connection terminals provided at an inner region of the mounting side surface for external connection reinforcement (where connection terminals 950, 952, 954 and 956 – Fig. 5F of Agahi-Kesheh et al. are shown extending into the inner region, where the terminal connections obviously provide external connection reinforcement).

Claim 11:

Where the connection terminals are connected to the grounding electrodes through corresponding via-holes in the multi-layer assembly (vias shown by Agahi-Kesheh et al. in Figs. 5A-F).

Claim 13:

Where at least one of the high-frequency terminals is located opposite to an inner electrode which forms the one of the high-frequency switching module comprised of the switching circuit and the filtering circuit, thus forming a capacitor circuit.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi-Kesheh et al. and Shapiro as applied to claim 1 above, and further in view of Zimmerman (U.S. Patent No. 6,137,062).

Claim 12:

Agahi-Kesheh et al. and Shapiro teach the high-frequency switching module (discussed above in the reasons for rejection of claim 1 above).

Agahi-Kesheh et al. and Shapiro do not teach where the high-frequency terminals are equipped with solder balls.

Zimmerman (Fig. 5A) shows a generic multi-layer package where the high-frequency terminals are equipped with solder balls comprising a well-known ball and grid (BGA) connection array.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the terminals of the high-frequency switching module disclosed by Agahi-Kesheh et al. and Shapiro with the BGA solder ball connection disclosed by Zimmerman. Such a modification would have realized the advantageous benefit of reducing the overall height of the ceramic package while providing high strength and reliable interconnection integrity (Zimmerman – col. 2, lines 4-14) thus suggesting the obviousness of the modification.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi-Kesheh et al. (U.S. Patent No. 5,513,382) and further in view of Tanaka et al. (U.S. Patent No. 6,445,262).

Claim 15:

Agahi-Kesheh et al. shows a high-frequency switching module primarily including a switching circuit (106 – Fig. 1) and filtering circuit (comprising elements 148, 158 and

164 forming a well-known pi filter within switching circuit 106, the circuits best illustrated in Figs. 1-3) comprising: a multi-layer assembly having a plurality of dielectric sheets of layers placed one over the other (Fig. 4); a plurality of high-frequency terminals provided on the outer surfaces of the multi-layer assembly (Fig. 5F); the switching circuit (142, 176 – Fig. 1) formed in the layers of the multi-layer assembly, having one end connected to a first high-frequency terminal (e.g. 142 connected to 112) of the plurality of high-frequency terminals; the filtering circuit (148 et al. – Fig. 1) formed in the layers of the multi-layer assembly, having one end connected to the other end of the switching circuit (124) and the other end connected to a second high-frequency terminal (218) of the plurality of high-frequency terminals, where a multi-layer capacitor forms a part of the switching circuit or filtering circuit

Agahi-Kesheh et al. does not show the well-known multi-layer capacitor which forms a part of the switching circuit is mounted on the multi-layer assembly.

Tanaka et al. shows a similar high-frequency switching module comprising a well-known art-recognized equivalent multi-layer capacitor (C23d and C23g – Fig. 5; obvious in that any high-frequency discrete chip capacitor would be a multi-layer capacitor since the capacitor would require two capacitive spaced plates, hence multi-layer) which forms a part of the switching circuit is mounted on the multi-layer assembly so that the direction of the stacking layers in the multi-layer assembly extends substantially vertical (vertical layers shown by Agahi-Kesheh et al.) to the direction of the stacking paired capacitor electrodes provided on layers of the multi-layer capacitor

(where the Examiner takes official notice that the layers of a discrete chip capacitor would have vertical stacking, i.e. well-known MLCC multi-layer chip capacitors).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the well-known multi-layer capacitor disclosed by Agahi-Kesheh et al. with the well-known art-recognized equivalent surface mounted capacitors disclosed by Tanaka et al. Such a modification would have been a mere substitution of well-known art-recognized equivalent capacitors, thus suggesting the obviousness of the modification.

Claim 16:

Where Tanaka et al. shows a top mounted chip inductor (L22d, g – Fig. 5; where the Examiner takes official notice that the layers of a discrete chip inductor would have vertical stacking, i.e. well-known MLCI multi-layer chip inductors).

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi-Kesheh et al. (U.S. Patent No. 5,513,382) and further in view of Ishizaki et al. (U.S. Patent No. 6,456,172).

Claim 17:

Agahi-Kesheh et al. shows a high-frequency switching module primarily including a switching circuit (306 – Fig. 3) and filtering circuit (comprising stripline 350 which is analogous to elements 148, 158 and 164 shown in Fig. 1, forming a well-known pi filter within switching circuit 306) comprising: a multi-layer assembly having a plurality of dielectric sheets of layers placed one over the other (Fig. 4); a plurality of high-

frequency terminals provided on the outer surfaces of the multi-layer assembly (Fig. 5F); the switching circuit (342, 376 – Fig. 3) formed in the layers of the multi-layer assembly, having one end connected to a first high-frequency terminal (e.g. 342 connected to 312) of the plurality of high-frequency terminals; the filtering circuit (350 - Fig. 3) formed in the layers of the multi-layer assembly, having one end connected to the other end of the switching circuit (324) and the other end connected to a second high-frequency terminal (318) of the plurality of high-frequency terminals, where a strip line forms a part of the switching circuit or filtering circuit (384 or 350 – Fig. 3).

Agahi-Kesheh et al. shows the well-known strip line in the multi-layer assembly but does not show the strip line partially in the multi-layer assembly while the remaining part of the strip line is located on a circuit board on which the multi-layer assembly is mounted on.

Ishizaki et al. (Fig. 7) shows a similar high-frequency switching module comprising a well-known art-recognized equivalent strip line partially in the multi-layer assembly while the remaining part of the strip line is located (L19, L20) on a circuit board on which the multi-layer assembly is mounted on.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the well-known strip line disclosed by Agahi-Kesheh et al. with the well-known art-recognized equivalent two piece strip line disclosed by Ishizaki et al. Such a modification would have been a mere substitution of well-known art-recognized equivalent capacitors, further in that the significance of the two piece strip line is not disclosed in the current invention thus would be made for the

same reasons as used in the current invention and shown by Ishizaki et al. thus suggesting the obviousness of the modification.

Claim 18:

Where the strip line is shown connected to the control terminal by both Agahi-Kesheh et al. (Fig. 3) and Ishizaki et al. (Fig. 7).

Allowable Subject Matter

Claims 6, 7, 9, 10, 14 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dean O Takaoka whose telephone number is (703) 305-6242. The examiner can normally be reached on 8:30a - 5:00p Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (703) 308-4909. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

dot
March 28, 2003

Robert Pascal
Supervisory Patent Examiner
Technology Center 2800